AMENDMENTS TO THE CLAIMS:

1. (Currently amended) A fixed point data generating circuit which receives a plurality of floating point data and which converts said plurality of floating point data into respective fixed point data, said fixed point data generating circuit comprising:

a reference data determining ~~means~~ unit which determines a reference floating point data from said plurality of floating point data;

an exponent part subtractor ~~means~~ unit which obtains a difference between each of the values of the exponent parts of said plurality of inputted floating point data and a value of an exponent part of said reference floating point data;

a shifting ~~means~~ unit which shifts a mantissa part of each of said plurality of floating point data by said difference obtained by said exponent part subtracting ~~means~~ unit; and

a bit extracting ~~means~~ unit which extracts a predetermined number of bits of said mantissa part shifted by said shifting ~~means~~ unit as fixed point data.

2. (Currently amended) A fixed point data generating circuit as set forth in claim 1, wherein said reference data determining ~~means is~~ unit comprises a maximum value detecting ~~means~~ circuit which detects the maximum value from among the values of said plurality of floating point data, and said reference floating point data is the ~~maximum data among said plurality of floating point~~ data having the detected maximum value.

3. (Currently amended) A fixed point data generating circuit as set forth in claim 1, wherein said reference data determining ~~means is~~ unit comprises a minimum value detecting ~~means~~

circuit which detects the minimum value from among the values of said plurality of floating point data, and said reference floating point data is the ~~minimum data among said plurality of floating point~~ data having the detected minimum value.

4. (Currently amended) A fixed point data generating circuit as set forth in claim 1, wherein said reference data determining ~~means is~~ unit comprises an average value calculating ~~means~~ circuit which calculates an average value of the values of said floating point data, and said reference floating point data is data having the average ~~data of said plurality of floating point data~~ value.

5. (Currently amended) A fixed point data generating circuit as set forth in claim 1, wherein said bit extracting ~~means~~ unit extracts bits as said fixed point data from a predetermined location.

6. (Currently amended) A fixed point data generating circuit as set forth in claim 1, wherein, when an overflow occurs in said bits extracted by said bit extracting ~~means~~ unit as said fixed point data, said bits extracted are caused to represent the maximum value. ~~thereby.~~

7. (Currently amended) A fixed point data generating circuit as set forth in claim 1, wherein, when an overflow occurs by shifting a mantissa part of each of said floating point data by said shifting ~~means~~ unit, shifted bits are caused to represent the maximum value. ~~thereby.~~

8. (Currently amended) A fixed point data generating circuit as set forth in claim 1, wherein said fixed point data extracted by said bit extracting ~~means~~ unit is inputted to a Viterbi decoder.

9. (Currently amended) A fixed point data generating circuit as set forth in claim 8, wherein the location of bits extracted by said bit extracting ~~means~~ unit as said fixed point data is previously determined to be a location having a high decoding rate.

10. (Currently amended) A computer-implemented method for generating fixed point data in which a plurality of floating point data are converted into respective fixed point data, said computer-implemented method comprising:

determining a reference floating point data from said plurality of floating point data;

obtaining a difference between each of the values of the exponent parts of said plurality of inputted floating point data and a value of an exponent part of said reference floating point data;

shifting a mantissa part of each of said plurality of floating point data by said difference between each of said values of said exponent parts of said plurality of inputted floating point data and ~~a~~ said value of ~~an~~ said exponent part of said reference floating point data; and

extracting a predetermined number of bits from said mantissa part shifted by said difference as fixed point data.

11. (Original) A method for generating fixed point data as set forth in claim 10, wherein said reference floating point data is the maximum data among said plurality of floating point data.

12. (Original) A method for generating fixed point data as set forth in claim 10, wherein said reference floating point data is the minimum data among said plurality of floating point data.

13. (Original) A method for generating fixed point data as set forth in claim 10, wherein said reference floating point data is the average data of said plurality of floating point data.

14. (Original) A method for generating fixed point data as set forth in claim 10, wherein, in said extracting a predetermined number of bits from said mantissa part shifted by said difference as said fixed point data, said bits are extracted from a predetermined location.

15. (Currently amended) A method for generating fixed point data as set forth in claim 10, wherein, in said extracting a predetermined number of bits from said mantissa part shifted by said difference as said fixed point data, when an overflow occurs in said bits extracted, said bits extracted are caused to represent the maximum value. ~~thereby.~~

16. (Currently amended) A method for generating fixed point data as set forth in claim 10, wherein, in said shifting a mantissa part of each of said floating point data by said difference, when an overflow occurs by shifting ~~a~~ said mantissa part of each of said floating point data, shifted bits are caused to represent the maximum value. ~~thereby.~~

17. (Original) A method for generating fixed point data as set forth in claim 10, wherein said fixed point data extracted in said extracting a predetermined number of bits from said mantissa part shifted by said difference is inputted to a Viterbi decoder.

18. (Currently amended) A method for generating fixed point data as set forth in claim 17, wherein the location of bits extracted in said extracting a predetermined number of bits from said mantissa part shifted by said difference is previously determined to be a location having a high decoding rate.

19. (New) A method for generating fixed point data as set forth in claim 10, further comprising utilizing the fixed point data.

20. (New) A method for generating fixed point data as set forth in claim 19, wherein the fixed point data is utilized in a Code Division Multiple Access system.